**Setting up the Devboard\_PowerMonitor**

This is a work in progress.

Sections.

1)3.3 Volt switch

2)Battery Recharge and Recharge Enable Switch

3)Powering the Device.

3)Programming the CPLD/FLASH

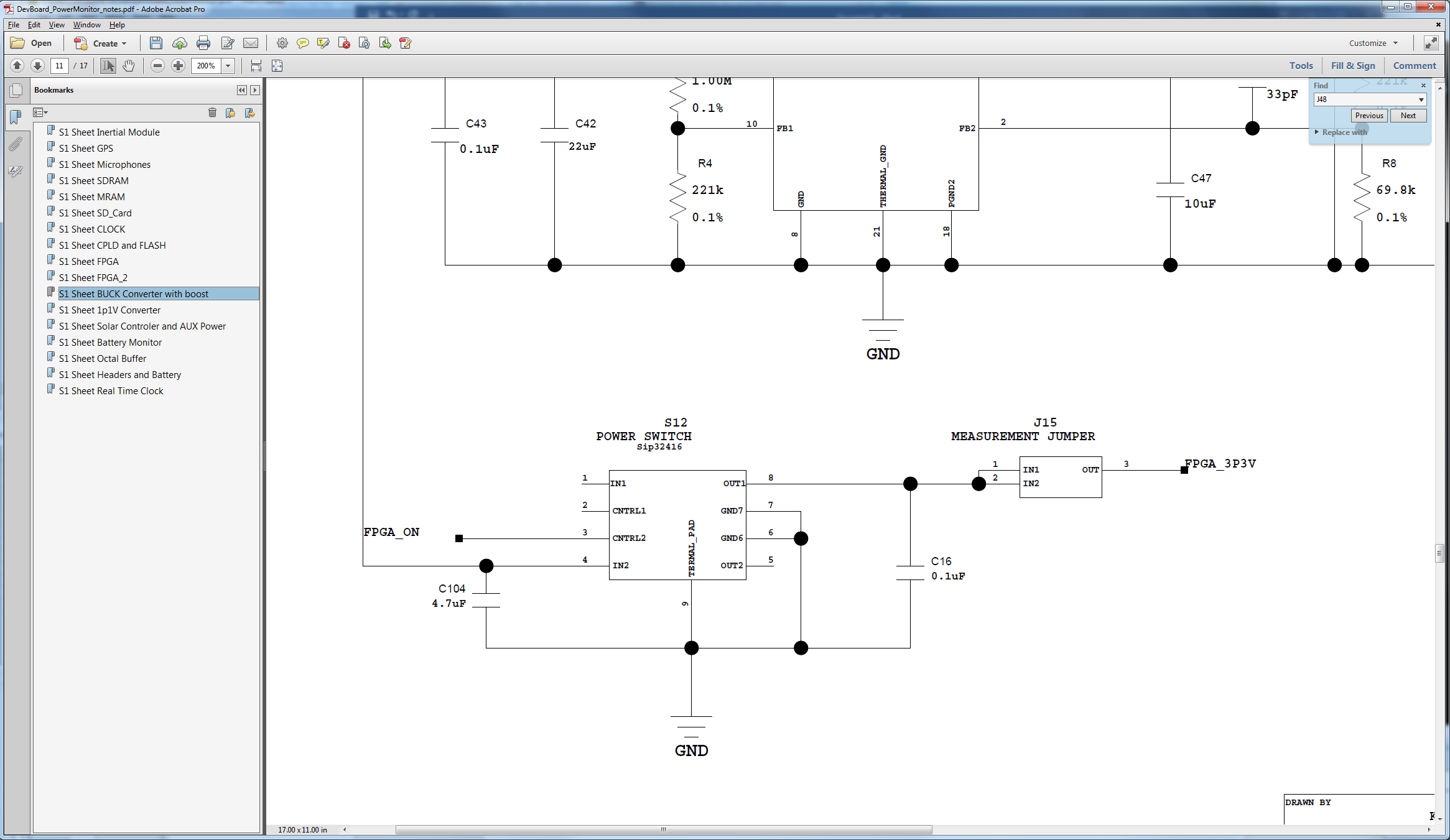
a) JTAG Jumping

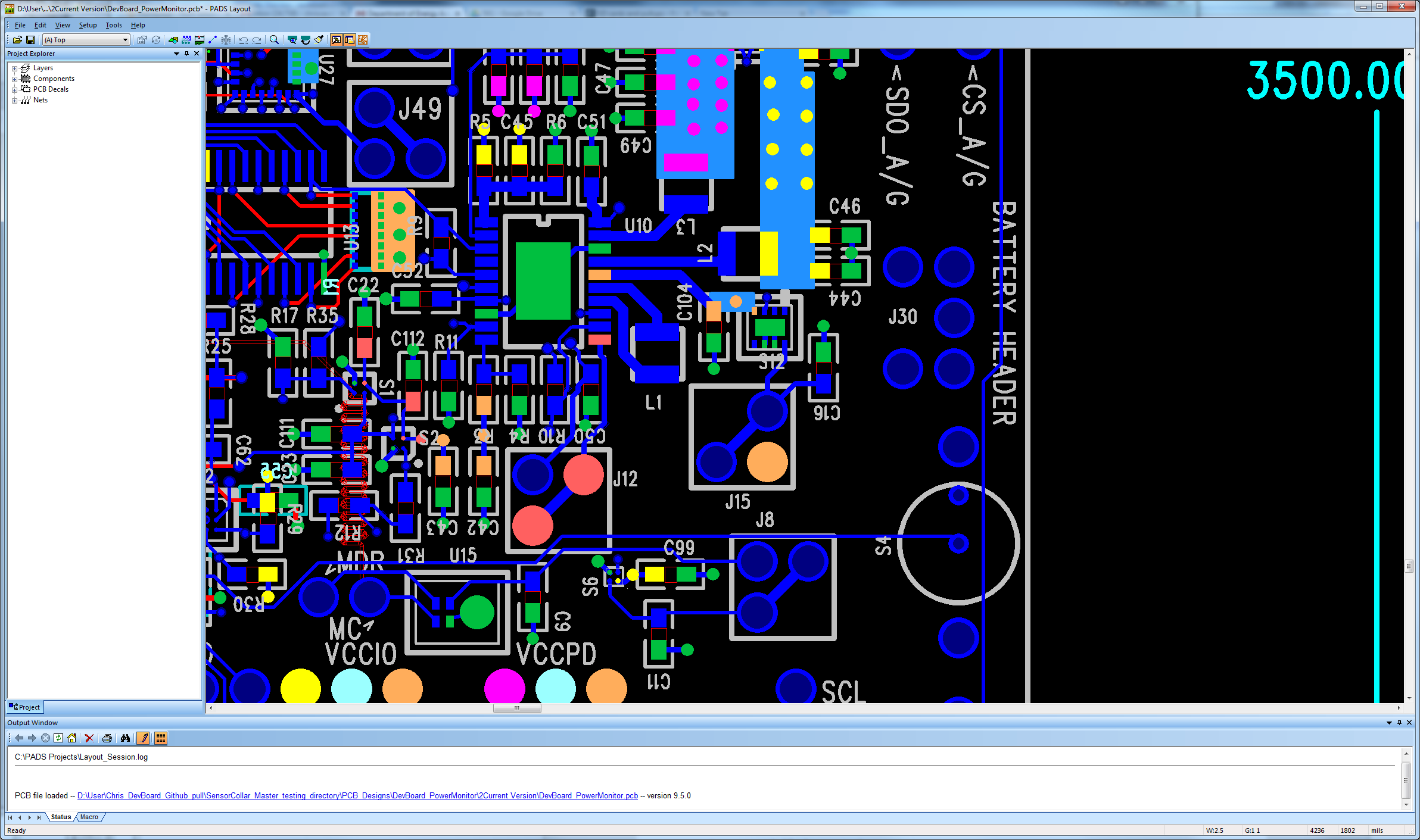
b) Programming correct images to CPLD and Flash

4)Botting and Programming the FPGA.

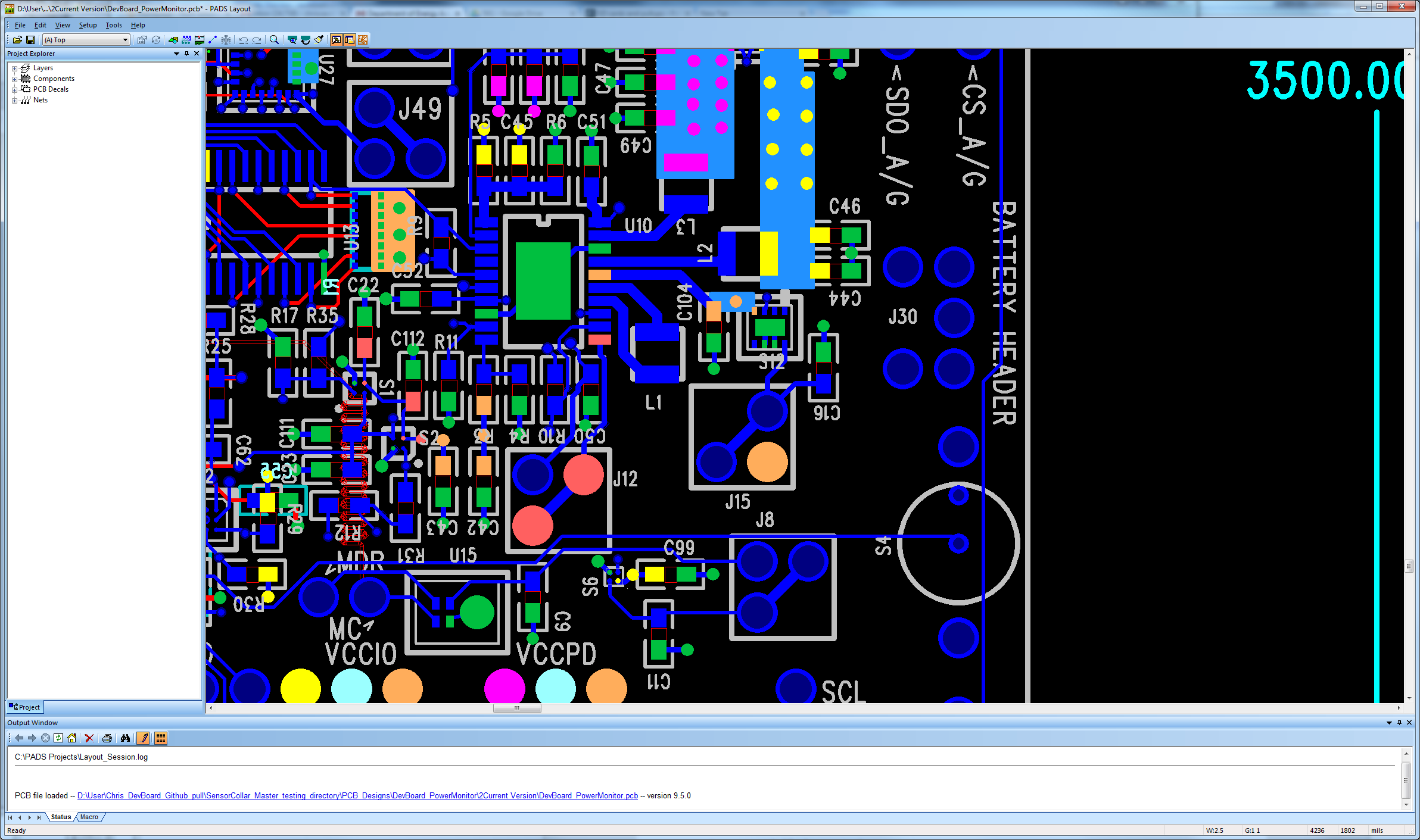
**1) 3.3 Volt Switch Fix**

The switch which controls the 3.3V rail which feeds the FPGA needs to be fixed. The switch is S12. The problem is that the control input and output do not match. Output 2 which is controlled is not tied anywhere.



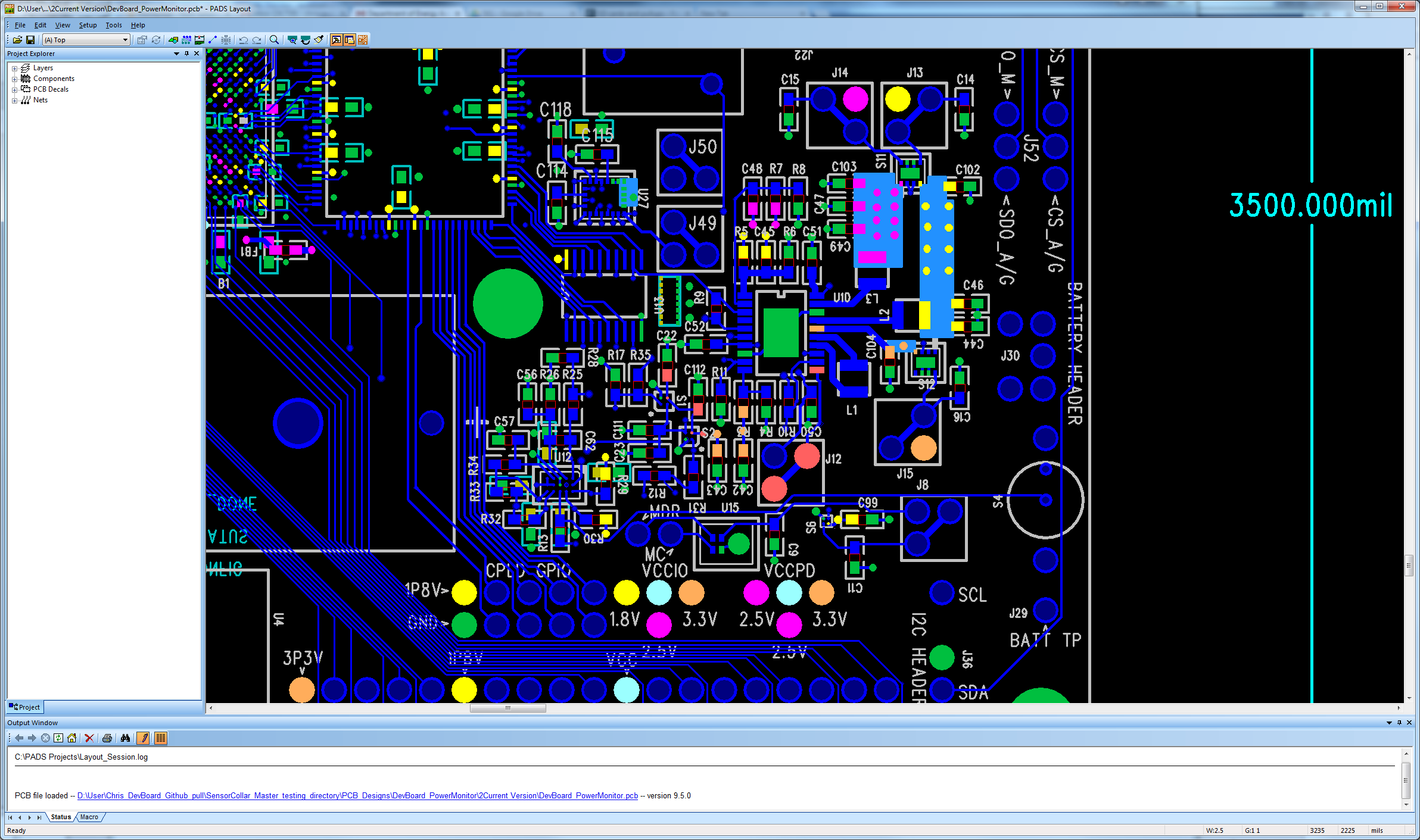


This is what needs to be physically done. Cut the trace at the dotted line. Insert a jumper wire as shown. I’m sure there are other solutions, this is what I did. You can also take out J15 completely and solder into those holes if that’s easier.



**2) S1 and S2 placed incorrectly. Pin 1 Placement Dot Incorrect. Decal Fine. Schematic Fine.**

Two switches on the board are placed incorrectly. If the switches are left in place, power is shorted to ground. You can either remove these switches or rotate them. If any battery testing is to be done on the board at a later time, these switches need to be rotated.



**Solution**

Either take the switches off with hot air or taken them off and rotate them 180 degrees. I’ve found you can do this without reapplying any paste or balls. They work after that.

**3) Powering the Device**

Jumpers needed for base operation:

J12 BuckBoost Input

J13 FPGA 1.8V

J14 FPGA 2.5V

J15 FPGA 3.3V

J21 Clock Power

J22 FPGA 1.1V

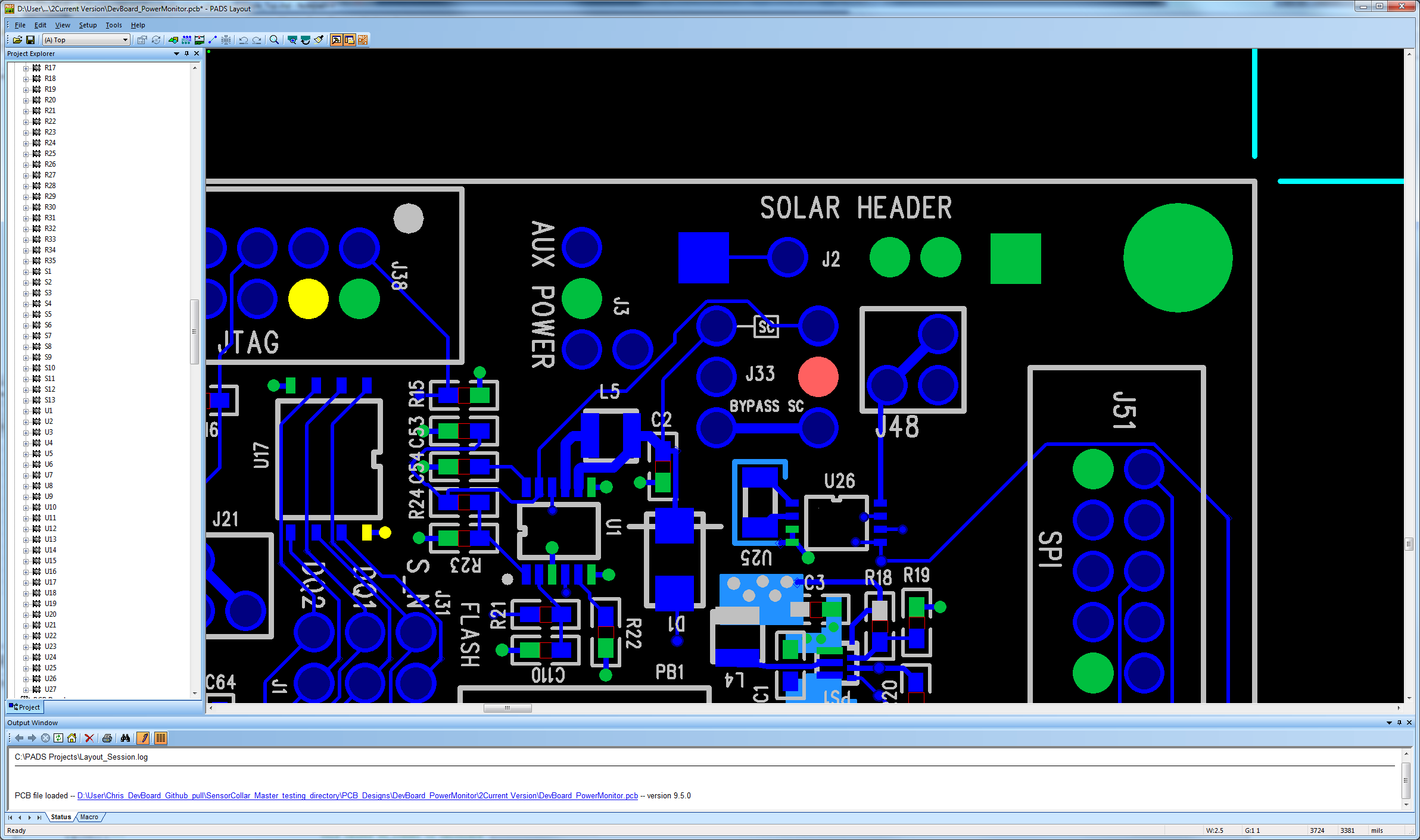
VCCIO and VCCPD Jumped 1.8V and 2.5V Respectively. Left Pin and Center Pin Jumped on both.

Bottom 2 sets of 2 at J33 Jumped. (Shown Below)

Any other devices you wish to work on need their associated power jumper.

Power should be applied as shown below at the solar header.

I strongly recommend current limiting your supply at first in case something goes wrong.

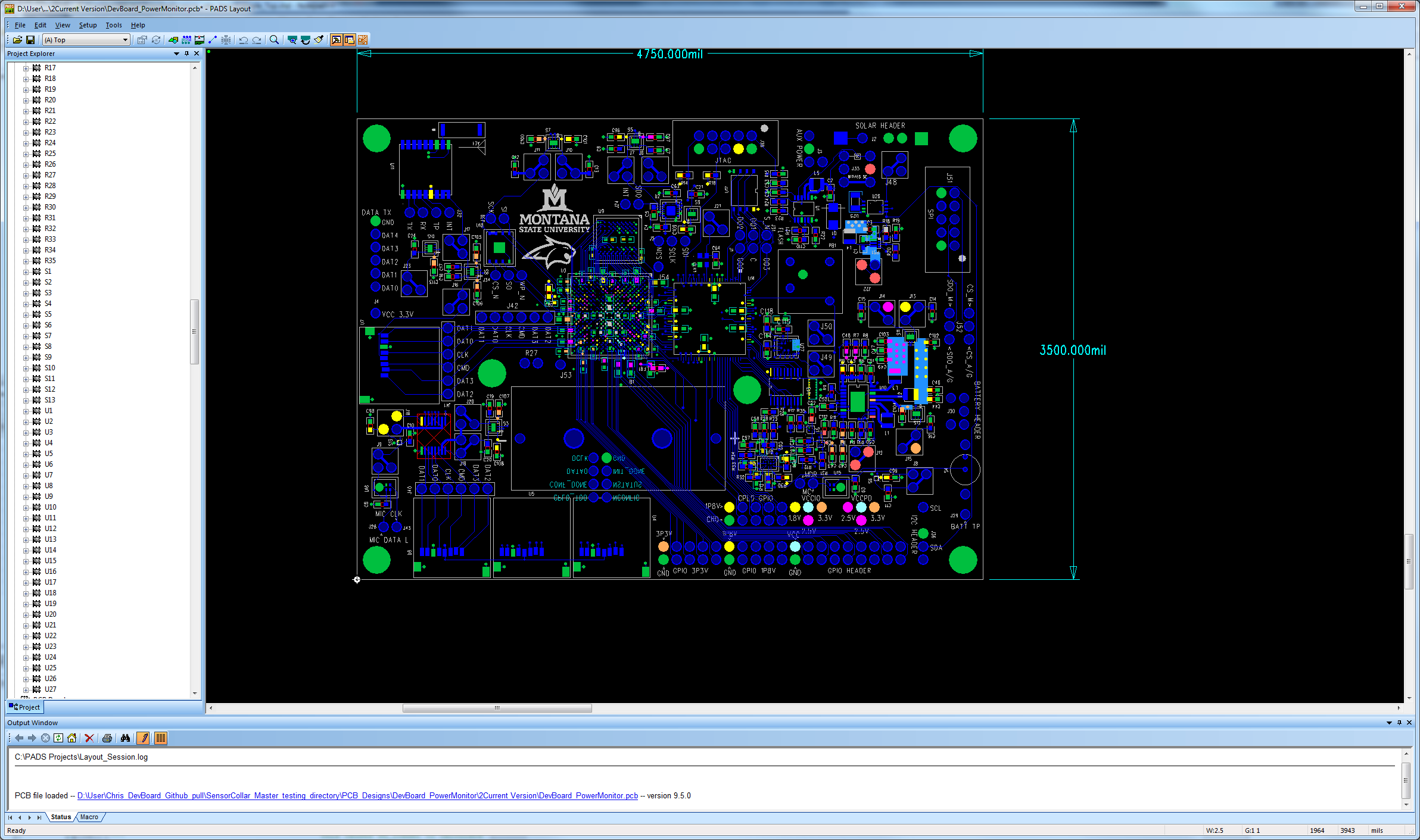


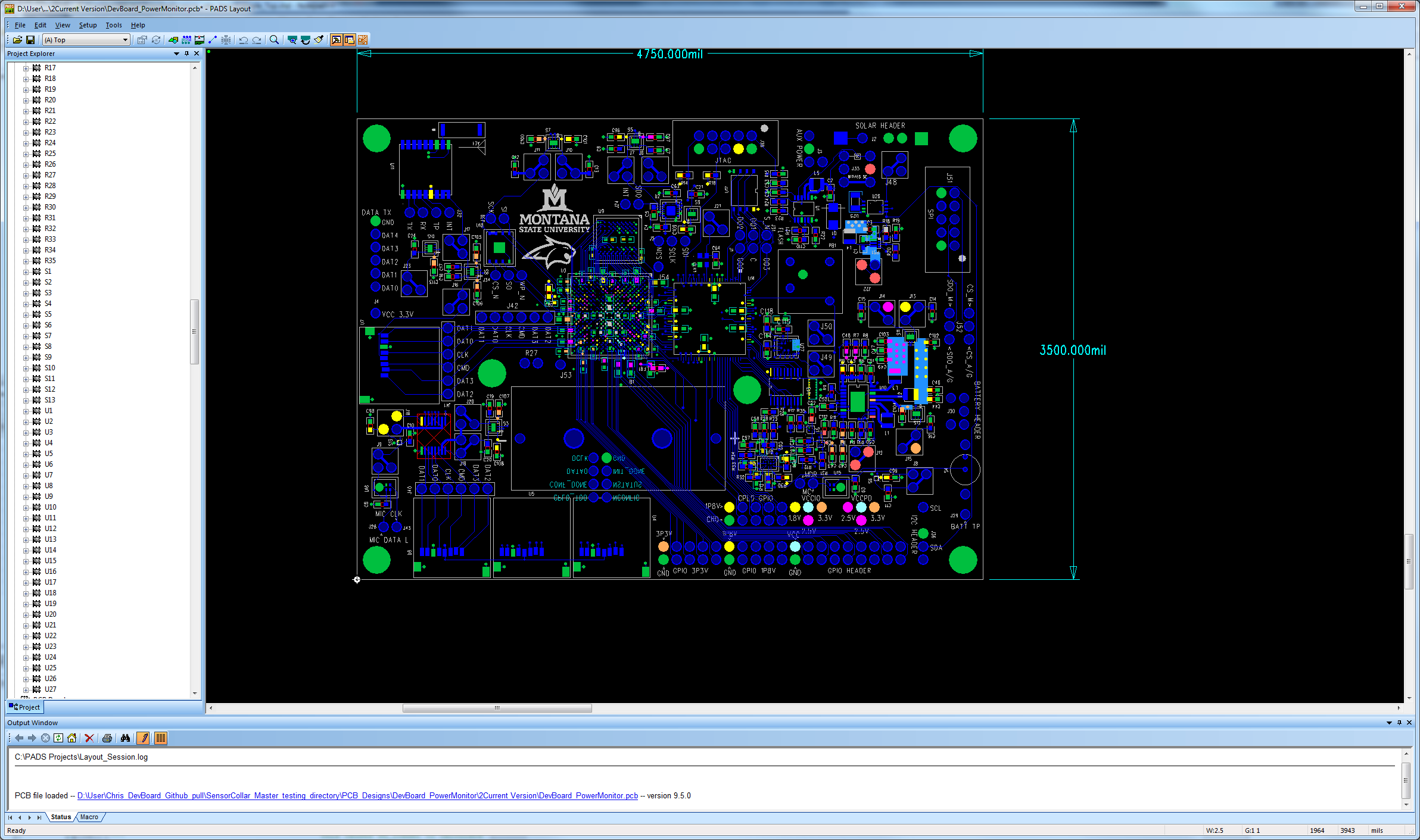
The buck boost needs >2.5V in. I recommend ~3.3V. However don’t exceed chip input max 5.5V. This configuration routes power onto power main and directly to the buck-boost regulator, bypassing the solar controller.

**3)Programming the CPLD/FLASH**

Due to the FPGA now routing its TDI to TDO when it is shut off, the JTAG chain is broken by default. To fix this two things need to be done

1) Jump CPLD\_TDO to TDO of the JTAG header.





2) Get 1.8V Power onto the JTAG VCC line.

I recommend jumping J13 to the CPLD GPIO 1.8V (Located near the bottom of the board.)

You should now be able to see the CPLD on the JTAG chain in Quartus when a USB Blaster is connected to the JTAG header. The ribbon cable lays away from the power board on the USB Blaster. Now we will load a CPLD image which will allow us to see and load the FLASH with an FPGA image.

Directories of Interest.

Source\_Code\DevBoard\_PowerMonitor\CPLD

Used for loading FPGA from Flash on Boot and Normal Operation

Source\_Code\DevBoard\_PowerMonitor\CPLD\_INIT

Used for loading Flash with FPGA image.

Source\_Code\DevBoard\_PowerMonitor\FPGA